

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket

RENERUS A. VAN DEN HEUVEL

NL 000674

Serial No.

Filed: CONCURRENTLY

METHOD FOR THE MANUFACTURE OF A SEMICONDUCTOR DEVICE WITH A
FIELD-EFFECT TRANSISTOR

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination,
please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

3. (Amended) A method as claimed in claim 1, characterised in that at the location of the source region (2) and the drain region (3) the gate oxide layer (4) is provided with an aperture (8,9) and that at the location of the aperture (8,9) the gate electrode (1) and the source region (2) and the drain region (3) are provided with a metal layer (11), which with the aid of the underlying silicon is converted into a silicide layer (11).

4. (Amended) A method as claimed in claim 1, characterised in that the distance from the drain region (3) to the gate electrode (1) is chosen between 1 and 4 μm .

5. (Amended) A method as claimed in claim 1, characterised in that on the gate electrode (1) an isolating layer (26) is deposited, on which a shielding electrode (27) is produced at the location of the gate electrode (1).

6. (Amended) A method as claimed in claim 1, characterised in that the spacers (5) are formed of a layer (5A) of silicon nitride.

7. (Amended) A method as claimed in claim 1, characterised in that the spacers (5) are formed of a layer of silicon nitride (5A) on which a layer (5B) of polycrystalline silicon is deposited.

8. (Amended) A method as claimed in claim 1, characterised in that additional semiconductor elements and preferably one or more passive components are integrated into the semiconductor body (10).

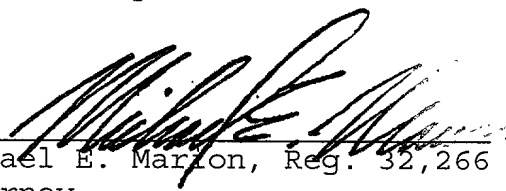
9. (Amended) A semiconductor device comprising a field-effect transistor obtained by means of a method as claimed in claim 1.

REMARKS

The foregoing amendments to claims 3-9, were made solely to avoid filing the claims in the multiple dependent form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights he may have under the Doctrine of Equivalents. Applicant furthermore reserves his right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

By 
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APPENDIX

3. (Amended) A method as claimed in claim 1 ~~or 2~~, characterised in that at the location of the source region (2) and the drain region (3) the gate oxide layer (4) is provided with an aperture (8,9) and that at the location of the aperture (8,9) the gate electrode (1) and the source region (2) and the drain region (3) are provided with a metal layer (11), which with the aid of the underlying silicon is converted into a silicide layer (11).

4. (Amended) A method as claimed in claim 1, ~~2 or 3~~, characterised in that the distance from the drain region (3) to the gate electrode (1) is chosen between 1 and 4 μm .

5. (Amended) A method as claimed in claim 1 ~~anyone of the above claims~~, characterised in that on the gate electrode (1) an isolating layer (26) is deposited, on which a shielding electrode (27) is produced at the location of the gate electrode (1).

6. (Amended) A method as claimed in claim 1 ~~anyone of the above claims~~, characterised in that the spacers (5) are formed of a layer (5A) of silicon nitride.

7. (Amended) A method as claimed in claim 1 ~~anyone of the above claims~~, characterised in that the spacers (5) are formed of a layer of silicon nitride (5A) on which a layer (5B) of polycrystalline silicon is deposited.

8. (Amended) A method as claimed in claim 1 ~~anyone of the above claims~~, characterised in that additional semiconductor elements and preferably one or more passive components are integrated into the semiconductor body (10).

